

67,200-1253
2003-1046

CONTACT STRUCTURE FOR NANOMETER CHARACTERISTIC DIMENSIONS

FIELD OF THE INVENTION

001 This invention generally relates to formation of nanometer scaled CMOS integrated circuits and more particularly to contact interconnect structures and method for forming the same to achieve reliable electrical contacts including to active contact regions in CMOS integrated circuits.

BACKGROUND OF THE INVENTION

002 Increasingly, integrated circuits require a higher density of device integration with increasingly shrinking characteristic dimensions, such dimensions referred to as deep sub-micron or nanometer technology where characteristic (critical) dimensions such as gate length are expected to soon decrease below 60 nm as well as below 45 nm. The decreasing characteristic dimensions of integrated circuits creates a host of new processing problems as well as design problems which must be overcome to successfully achieve higher levels of integration.

003 Contact interconnects, also referred to as vias, are particularly critical for making contact with active areas of a transistor device including active contact regions such as the

67,200-1253
2003-1046

gate electrode and source and drain (S/D) regions. For example, as characteristic dimensions of transistor devices are scaled down to deep submicron dimensions, the contact opening width allowable is increasingly limited due to the shrinking size of the contact areas. Conventional processing steps such as photolithography and reactive ion etching have increasingly limited process windows in order to make reliable contacts while the shortcomings of inadequate etching bias, etching profiles, premature etch stop, unintentional overetching of contact regions, and etch opening misalignment.

004 For example, in prior art processes, a metal filled contact interconnect or via have been used to make contact from the active contact regions including gate electrode and S/D regions to the first metallization layer through a single Interlayer-dielectric (ILD) layer, also referred to as a pre-metal dielectric (PMD) layer. In prior art approaches, The ILD layer is formed overlying the active devices followed by formation of metal filled contacts extending through the ILD layer thickness to electrically connect the active regions to an overlying metallization layer which begins the formation of wiring circuitry formed in multiple overlying metallization levels.

67,200-1253
2003-1046

005 Due to signal delay concerns and IC design rules, the size of active contact regions in a scaling down process shrinks significantly faster than the thickness of the ILD layer, due to a desire to prevent stray capacitance from the metallization layer to the gate structure. As a result, contact interconnects must be formed with increasingly high aspect ratios which creates processing difficulties such as inadequate etching biases and profiles, premature etch stop, inadequate metal filling coverage, unintentional overetching into the contact regions, as well as inadequate lithography resolution due to the required thickness of resist layers when used as etching masks in high aspect ratio plasma etching process.

006 These and other shortcomings demonstrate a need in the semiconductor device integrated circuit manufacturing art for improved contact interconnects structures and a method for forming the same to form more reliable contact interconnects having smaller width dimensions while avoiding the various shortcomings of the prior art.

007 It is therefore an object of the present invention to provide improved contact interconnects structures and a method for forming the same to form more reliable contact interconnects

67,200-1253
2003-1046

having smaller width dimensions while avoiding the various shortcomings of the prior art.

SUMMARY OF THE INVENTION

008 To achieve the foregoing and other objects, and in accordance with the purposes of the present invention, as embodied and broadly described herein, the present invention provides a contact interconnect structure and method for forming the same to achieve improved patterning, etching and metal filling characteristics.

009 In a first embodiment, the method includes providing a semiconductor substrate including CMOS devices including active contact regions; forming a first set of dielectric layers to form a first thickness for etching a first set of openings through a thickness thereof including a bottom portion having a maximum width of less than about 70 nanometers; etching the first set of openings to contact active contact regions; filling the first set of openings with a first metal; forming a second set of dielectric layers to form a second thickness for etching a second set of openings through the second thickness comprising a bottom portion having a maximum width of less than about 70 nanometers; etching the second set of openings to provide electrical

67,200-1253
2003-1046

communication with the first set of openings; and, filling the second set of openings with a second metal to form contact interconnects.

0010 These and other embodiments, aspects and features of the invention will be better understood from a detailed description of the preferred embodiments of the invention which are further described below in conjunction with the accompanying Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

0011 Figures 1A-1E are cross sectional schematic representations of exemplary portions of an integrated circuit semiconductor device at stages of manufacture according to an embodiment of the present invention.

0012 Figure 2 is an exemplary process flow diagram including several embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

0013 Although the method of the present invention is explained with reference to an exemplary CMOS transistor and shallow trench isolation (STI) structures, it will be appreciated that the shallow contact interconnects and method of forming the same may

67,200-1253
2003-1046

be applied in general to forming contact interconnects where an integrated circuit device or process may be improved by forming contact interconnects in a multi-step process to overcome processing issues and device performance issues related to forming high aspect ratio damascene openings. In addition, it will be appreciated that while the device and method of the present invention is particularly advantageously used for forming integrated circuit devices with characteristic dimensions (e.g., gate lengths) less than about 60 nm, including less than about 45 nm, that the method and structure may be used in forming larger characteristic dimension devices.

0014 Referring to Figures 1A-1E in an exemplary embodiment of the method of the present invention, are shown cross-sectional schematic views of a portion of a semiconductor wafer during stages in production of a CMOS integrated circuit, for example FET transistor devices 10A, 10B, and 10C, forming a portion of logic or memory IC circuits. For example, referring to Figure 1A is shown a semiconductor substrate 12 including an active regions including channel regions 12A, 12B, and 12C where the active regions are electrically isolated by isolation regions, preferably shallow trench isolation (STI) structures, e.g., 13A, 13B, and 13C which are formed by conventional methods including

67,200-1253
2003-1046

backfilling an STI trench formed in the semiconductor substrate with an oxide dielectric, for example TEOS oxide. It will be appreciated that other methods for achieving electrical isolation may be used including LOCOS, field oxide, and silicon on insulator (SOI).

0015 CMOS devices (e.g., FET transistors) 10A, 10B, 10C may form a portion of a logic or memory circuit and may be formed by conventional methods with conventional materials including first conductive active contact regions e.g., 14, for example formed over source/drain regions. The CMOS devices include respective gate structures which include conventional gate dielectric portions e.g., 16 and respective overly gate electrode portions e.g., 18C. In addition, the respective gates structures include pairs of offset spacers e.g., 20 on either side of the gate structures formed of silicon oxide, silicon nitride, silicon oxynitride or combinations thereof. The semiconductor substrate 12 may be formed of silicon, silicon on insulator (SOI), strained silicon, and silicon-germanium (SiGe), or combinations thereof.

0016 Still referring to Figure 1A, the gate structures including gate dielectric portions may be formed by conventional CVD deposition, lithographic patterning, and plasma and/or wet

67,200-1253
2003-1046

etching methods known in the art. The gate dielectric may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, or chemical vapor deposition. Silicon oxide, silicon nitride, silicon oxynitride, high-K (e.g., $K > 8$) dielectrics including transition metal oxide and rare earth oxides may be used for the gate dielectrics.

0017 The gate electrode portion e.g., 18A, 18B, 18C of the gate structure may be formed of polysilicon, polysilicon-germanium, metals, metal silicides, metal nitrides, or conductive metal oxides. Second conductive active contact regions e.g., 19 are optionally formed in the uppermost portion of the gate electrodes along with first conductive contact regions e.g., 14 by conventional CVD or sputtering methods including silicidation to form self-aligned silicides a/s is known in the art. Preferably, the first and second active contact regions include one or a combination of conductive materials such as metals, such as Ti, Co, Ni, Pt, W and silicides thereof, e.g., TiSi_2 , CoSi_2 , NiSi , PtSi , WSi_2 , as well as metal nitrides such as TiN and TaN , or combinations of the foregoing.

67,200-1253
2003-1046

0018 For example, the gate dielectric is first formed by CVD, sputtering or thermal growth processes followed by deposition of an overlying gate electrode material and a hardmask layer. Conventional Lithographic patterning and dry etching are then carried out to form the gate structure. A first ion implant is carried out to form doped regions (not shown) in the semiconductor substrate e.g., SDE regions adjacent both sides of the gate structures followed by a thermal activation process. One or more spacer dielectric layers are then formed e.g., LPCVD or PECVD deposition followed by a wet and/or dry etchback to form the offset spacers e.g., 20. A second higher dose ion implant is then carried out to form more highly doped S/D regions on either side of the gate structures using the offset spacers as an implant mask. First and second conductive contact regions, e.g., e.g., 14 and 19 are then formed using the preferred materials outlined above.

0019 Referring to Figure 1B, according to an important aspect of the invention, a first insulating dielectric (ILD) layer e.g., 22A is blanket deposited by conventional methods, e.g., LPCVD, PECVD over the process surface, followed by a conventional planarization process such as CMP. Preferably, the first ILD

67,200-1253
2003-1046

layer 22A is formed of one or a combinations of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, SiC, nitrogen doped silicon oxide, silicon nitride (e.g., Si_3N_4), silicon oxynitride (e.g., SiON), low-K ($K < 2.9$) or high-K ($K > 5$) dielectrics, and fluorine doped silicon oxide (e.g., FSG). In one embodiment, the first ILD layer 22A is deposited in a two step process to form a first lower contact etch stop layer portion 22AA including one or combinations of, SiC, nitrogen doped silicon oxide, silicon nitride (e.g., Si_3N_4), and silicon oxynitride (e.g., SiON) followed by deposition of and an upper portion including one or combinations of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, low-K ($K < 2.9$) or high-K ($K > 5$) dielectrics, and fluorine doped silicon oxide (e.g., FSG).

0020 In a critical aspect of the present invention, the preferred thickness of the first dielectric layer will depend on the maximum thickness of the bottom portion of a contact opening subsequently desired to be formed and a maximum aspect ratio of the contact opening desired to enable improved contact opening etching and metal coverage in a contact metal filling process to improve device performance and reliability as explained further below.

67,200-1253
2003-1046

0021 Preferably, the aspect ratio, defined herein as the contact opening depth/ contact opening width at the bottom portion of the contact opening, is preferably less than about 3.3 with the contact opening width at the bottom portion of the contact hole being less than about 70 nm. Thus the thickness of the first ILD layer following planarization including optional deposition of one or more of a hardmask layers and overlying inorganic or organic anti-reflectance (ARC) coatings, is preferably less than about 2350 Angstroms to form with the preferred contact opening aspect ratio. More preferably, the aspect ratio for the contact hole formed in the first ILD layer is less than about 4.5 with a contact opening width (bottom portion) less than about 50 nm.

0022 In an exemplary embodiment, a hardmask layer 24A such as SiC, Si₃N₄, SiO_xN_y (e.g. SiON) is first formed, e.g., blanket deposited over ILD layer 22A by a conventional CVD method.

0023 Referring to Figure 1C, following formation of an inorganic or organic ARC layer 24B one or more resist layers e.g., 26 is deposited and patterned. The resist layer 26 may be a single or multiple layer resist including organic and inorganic materials, for example a lower organic rest layer and an

67,200-1253
2003-1046

overlying resist including silicon incorporated by a silylation process or including silicon monomers. The resist layer e.g., 26 may have a total thickness of about 0.1 microns to about 1.0 microns, and is preferably sensitive to wavelengths less than about 400 nm. A lithographic patterning process is carried out including radiation exposure and development by appropriate wet or dry development processes, followed by conventional dry etching processes to etch through the first ILD layer 22A to form a first set of contact openings e.g., 28A, 28B, 28C, 28D, and 28E. The contact openings may be formed in the shape of an oval (circular), butt contact, rectangular (e.g., square), or combinations thereof. For example, the contact openings may include a local interconnect opening, e.g., 28C, having the preferred aspect ratio at a lowermost (bottom) portion of the contact opening.

0024 Referring to Figure 1D, following removal of the resist layers, the contact openings are filled with a metal by conventional processes, including barrier layer formation, where the filling metal preferably includes Cu, W, Al, AlCu, TiN, TiW, Ti, TaN, Ta, or combination thereof. Following metal filling, a planarization process, such as metal etchback or CMP is carried

67,200-1253
2003-1046

out to planarize the metal filled openings to form metal filled contact interconnects e.g., 30A, 30B, 30C, 30D, and 30E.

0025 Referring to Figure 1E, according to an important and critical aspect of the invention, at least a second insulating dielectric (ILD) layer e.g., 22B is formed over the first ILD layer 22A such that the first and second (or more) dielectric insulating layers is sufficient to meet a required design thickness to meet a required capacitance. For example, the second ILD layer is formed by blanket depositing by conventional methods, e.g., LPCVD, PECVD one or more dielectric layers over the first ILD layer 22A followed by a conventional planarization process such as CMP. Preferably, the second ILD layer 22B is preferably formed in the same manner and using the same preferred materials as the first ILD layer 22A. In one embodiment, the second dielectric layer 22B is deposited in a two step process to form a first lower portion, e.g., a contact etch stop layer, 22BB including one or a combination of SiC, nitrogen doped silicon oxide, silicon nitride (e.g., Si_3N_4), and silicon oxynitride (e.g., SiON) and an upper portion 22B including one or a combination of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, low-K ($K < 2.9$) or high-K ($K > 5$) dielectrics, and fluorine doped silicon oxide (e.g., FSG). In the exemplary embodiment preferably one or

67,200-1253
2003-1046

more of a hardmask layer 24C and an ARC layer 24D are formed over the ILD layer 22B according to the same preferred embodiments outlines for hardmask layer 24A and ARC layer 24B.

0026 Referring to Figure 1F, a similar process as outlined for forming the first set of contact interconnects 30A, 30B, 30C, 30D, and 30E is then carried out to form a second set of contact interconnects e.g., 32A, 32B, and 32C extending through the thickness of the second ILD layer 22B to make contact (e.g., including overlying and at least partially encompassing) portions of the first set of contact interconnects. The second set of contact interconnects is formed according to the same preferred embodiments and aspect ratios as the first set of contact interconnects the first ILD layer 22A. The second set of contact interconnects may have the same or different preferred aspect ratio as the second set of contact interconnects, for example having a smaller aspect ratio to ensure adequate interconnect overlap. In addition, longer (horizontal to the substrate) contact interconnects e.g., 32A may be formed to conductively connect one or more of the first set of contact openings e.g., 30A and 30B. Preferably, the length of the longer contact interconnects, e.g., 32A is between about 0.15 microns and about 500 microns.

67,200-1253
2003-1046

0027 Although not shown, conventional overlying metallization layers are then formed to make electrical contact with the second set of contact interconnects. It will be appreciated that multiple overlying dielectric layers and metallization interconnects may be subsequently formed to form multiple metallization levels overlying the first and second ILD layers.

0028 Advantageously, according to the present invention, by forming contact interconnects in a multi-step process, for example, including at least two ILD layers with contact interconnects formed therein, electrical contact from the first overlying metallization layer to active device regions is improved. By sequentially forming contact openings followed by metal filling processes, in multiple ILD layers, the critical design requirements of forming contact openings having a bottom portion with a width of less than about 70 nm, more preferably less than about 50 nm, are able to be reliably formed in contrast with prior art processes. Included among the advantages of the present invention, is the creation of larger etch process window, leading to formation of accurately aligned, cleanly etched, and adequate metal coverage of small width contacts thereby forming more reliable contacts with improved performance to the active

67,200-1253
2003-1046

regions. The multi-step process allows the formation of larger aspect ratio openings in contrast with prior art processes. Other added benefits include improved ILD gap filling due to thinner contact etch stop layers and improve lithographic resolution due to thinner photoresist layers. In short, the reliability and accuracy of forming contact interconnects is improved allowing processes to be scaled down to include devices with critical dimensions (CD) of less than about 45 nm (e.g. gate length).

0029 Referring to Figure 2 is a process flow diagram including several embodiments of the present invention. In process 201, a semiconductor substrate including CMOS transistor devices is provided including active contact regions according to preferred embodiments. In process 203 a first ILD layer (including multiple dielectric layers) is formed to a first planarized thickness. In process 205, a first set of contact interconnects with critical widths and aspect ratios are formed in the first ILD layer to contact one or more of the active contact regions. In process 207, a second ILD layer (including multiple layers) is formed to a second planarized thickness. In process 209, a second set of contact interconnects with critical widths and aspect ratios are formed in the second ILD layer to contact one

67,200-1253
2003-1046

or more of the first contact interconnects. In process 211, an overlying metallization level including a metallization interconnects is formed to contact on or more of the second contact interconnects.

0030 The preferred embodiments, aspects, and features of the invention having been described, it will be apparent to those skilled in the art that numerous variations, modifications, and substitutions may be made without departing from the spirit of the invention as disclosed and further claimed below.